

Attorney Docket No. 10559-270001
Application No. 09/675,816
Amendment dated June 1, 2004
Reply to Office Action dated January 29, 2004

Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Previously presented) A method of handling instructions within a processor comprising:

decoding at least a portion of an instruction to determine a first destination and a second destination of the instruction;

re-encoding only a portion of the instruction to a second re-encoded code used for said first destination and forwarding the re-encoded instruction to said first destination; and

forwarding a different portion of the instruction, without re-encoding, to said second destination.

2. (Canceled)

3. (Previously presented) The method of Claim 1, wherein said first destination is a first functional unit which operates based on op codes.

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4. (Previously presented) The method of Claim 3, further comprising sending at least a portion of the decoded instruction to a second functional unit which operates based on decoded information.

5. (Original) The method of Claim 1, further comprising determining a portion of the coded instruction to decode.

6. (Canceled)

7. (Original) The method of Claim 1, further comprising handling instructions in a digital signal processor.

8. (Previously presented) A method of processing instructions within a processor comprising:
receiving a coded processor instruction;
determining a first functional unit which operates based on coded instructions, a second functional unit which operates based on decoded information obtained from the coded instruction, and a third functional unit, which each receive parts of the instruction;

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forwarding a first portion of the coded instruction having a first destination location representing the first functional unit, to the first functional unit;

decoding another portion of the instruction;

forwarding said another portion of the decoded instruction having a second destination location representing the second functional unit, to the second functional unit;

re-encoding any remaining portion of the instruction to a second code; and

forwarding the re-encoded instruction to a third location representing the third functional unit.

9. (Canceled)

10. (Previously presented) The method of Claim 8, wherein said second functional unit is a data address generator.

11. (Previously presented) The method of Claim 8, wherein the third functional unit is a system pipe.

12. (Original) The method of Claim 8, further comprising processing instructions within a digital signal processor.

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13. (Original) The method of Claim 8, further comprising decoding and re-encoding with a decoder.

14. (Previously presented) A processor comprising:
a decoder which receives an instruction coded in a first code and decodes at least a portion of the instruction to determine a first destination and a second destination of the instruction and forwards a portion of the instruction to said first destination, which operates based on a decoded code; an encoder which re-encodes a portion of the instruction to a second encoded code used for said second destination.

15. (Original) The processor of Claim 14, wherein the decoder determines the destination of the instruction.

16. (Original) The processor of Claim 15, wherein the decoder forwards control signals to other portions of the processor.

17. (Original) The processor of Claim 16, wherein the control signals may be in the first code or the second code.

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18. (Original) The processor of Claim 14, wherein the processor is a digital signal processor.